

IN THE CLAIMS

What is claimed is:

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1. 1. A programmable logic device assembly, comprising:
 2. a programmable logic circuit that provides functions according to configuration data including a self-test function; and
 4. at least one nonvolatile store coupled to the programmable logic circuit that provides self-test configuration data for the programmable logic circuit
 5. and can subsequently store user configuration data.
 1. 2. The programmable logic device assembly of claim 1, wherein:
 2. the programmable circuit can provide a self-test result when configured for self-test function.
 1. 3. The programmable logic device assembly of claim 2, further including:
 2. a test port for providing the self-test result in a predetermined format.
 1. 4. The programmable logic device assembly of claim 1, wherein:
 2. the at least one nonvolatile store includes a first nonvolatile store formed with the programmable logic circuit on a single integrated circuit die.
 1. 5. The programmable logic device assembly of claim 4, wherein:
 2. the first nonvolatile store includes re-programmable nonvolatile circuit

3 elements.

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3 6. The programmable logic device assembly of claim 5, wherein:
the first nonvolatile store includes electrically erasable programmable
read-only-memory cells.

1 7. The programmable logic device assembly of claim 4, wherein:
2 the self-test configuration data in the at least one nonvolatile store is
3 set by at least one manufacturing process step.

1 8. The programmable logic device assembly of claim 7, wherein:
2 the at least one nonvolatile store includes a mask programmable read-
3 only-memory that stored self-test configuration data and a separate
4 nonvolatile memory that can store user configuration data.

1 9. The programmable logic device assembly of claim 1, wherein:
2 the at least one nonvolatile store includes at least two sectors and self-
3 test configuration data is stored in a first sector.

1 10. The programmable logic device assembly of claim 9, wherein:
2 the first sector is a boot sector.

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1 11. A method, comprising the steps of:
2 performing a self-test on a programmable logic circuit according to
3 self-test configuration data in a self-test nonvolatile store; and
4 storing user configuration data in a user nonvolatile store if the
5 programmable logic circuit passes the self-test.

1 12. The method of claim 11, wherein:
2 the self-test nonvolatile store is the same as the user nonvolatile store.

1 13. The method of claim 12, wherein:
2 storing user configuration data includes programming user
3 configuration data in locations that stored self-test configuration data.

1 14. The method of claim 12, wherein:
2 storing user configuration data includes programming user
3 configuration data in locations that are different than those that store self-test
4 configuration data.

1 15. The method of claim 11, further including:
2 forming the self-test nonvolatile on the same die as the programmable
3 logic circuit.

1 16. The method of claim 11, further including:

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ale assembling the programmable logic circuit one die with the
3 nonvolatile store on another die into one package.

1 17. The programmable logic circuit of claim 16, wherein:
2 the one package is a multi-chip module.

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1 18. A programmable logic self-test method, comprising the steps of:
2 storing self-test information in a first nonvolatile store that places a
3 programmable logic circuit into a self-test configuration;
4 executing a self-test on the programmable logic circuit; and
5 providing user configuration information that places the programmable
6 logic circuit in a user configuration.

1 19. The method of claim 18, wherein:
2 the user configuration data is stored in the first nonvolatile store.

1 20. The method of p claim 18, wherein:
2 the user configuration data is stored in a second nonvolatile store that
3 is different than the first nonvolatile store.